REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Office Action dated 3 October 2007. Responsive to that Office Action, Claim 1 has been amended further clarify its recitations.

In the Office Action, the Examiner rejected Claims 1-23 under 35 U.S.C. 102(b) as being anticipated by the Lowe, et al. reference. In setting forth the rejection, the Examiner cited Lowe, et al.'s Fig. 8 and the passage at col. 2, lines 2-15, of its specification for teaching VHDL models of various computer system components stored in a configuration interpretation mechanism, from which the user may choose for compilation prior to run-time simulation. The Examiner further cited cols. 18 and 19, lines 58-67 and 1-20 of the Lowe, et al. specification for disclosing the automatic generation of tests based on a selected scenario.

As newly-amended independent Claim 1 clearly recites, Applicants' method includes among its combinations of features "automatically generating at least one test" for a device under test (DUT). The test itself is automatically generated "from ... at least one selected scenario" so as "to provide at least one input for driving simulated operation of the DUT," as Claim 1 now even more clearly recites.

The full combinations of these and other features now more clearly recited by the pending Claims is nowhere disclosed by Lowe, et al. While that reference is directed to dynamic verification of a DUT, its focus and fundamental approach

are entirely different. Note that Lowe, et al. sets out to enable different "permutations" of a test, so that the same test may be transparently applied to any one of numerous test configurations.

Contemplating the various testing configurations determined by such factors as the amount of memory populating the system, number of memory banks, types of memory, addresses of PCI bus masters/slaves, external device modes, processor types, and the like (see column 19; lines 34-39) in a given situation, Lowe, et al. provides for "a configuration-independent test suite" (column 19; lines 27-28) – not by adapting the test – but by adapting the software model of the device under test itself. The particularities of the test configuration at hand are interpreted at block 804, then the software model "of the computer system component being tested" is accordingly compiled prior to the simulation at block 806 (column 20; lines 8-9) such that it suits the given test configuration. Thus, Lowe, et al. neither generates nor modifies the test itself, but updates instead the DUT model as required by the test configuration. This teaches flatly away from "automatically generating the test," as Claim 1 recites, let alone from such automatic test generation in the manner fully claimed.

This fact is underscored all the more by Lowe, et al.'s emphatic specification more than once that it realizes the "configuration-independent test suite" in a versatile and simple manner by ensuring that test "configuration and bus stimulus are separated," such that:

> As shown [in Fig. 8], the test stimulus (block 807) and the functionality verification of the device under test (block 809) are performed in a manner that is independent of the test configuration selected under step 804.

(Column 19; lines 44-48; *emphasis added*).

Thus, to whatever extent automation may be accorded to the process of test configuration selection and subsequent adaptation of the DUT model, such automation simply does not constitute "automatically generating ...[a] test," which "provide[s] at least one input for driving simulated operation of the DUT," newly-amended Claim 1 now even further clarifies. Indeed, Lowe, et al. specifically prescribes that "the user selects a test configuration through appropriate VHDL models from the configuration interpretation mechanism (block 804)," (column 20; lines 5-8).

Lowe, et al. specifies in connection with the example shown in Fig. 9, moreover, that "a stimulus from the stimulus file" forms the reference signal shown there, and that this "reference signal is preferably user-defined," (column 20; line 32). This hardly teaches the "automatic[ ] generating" of the test recited in the pending Claims.

It is respectfully submitted, therefore, that the cited Lowe, et al. reference fails to disclose the unique combinations of elements recited by the pending Claims for the purposes and objectives disclosed in the subject Patent Application.

It is now believed that the subject Patent Application has been placed fully in condition for allowance, and such action is respectfully requested.

No fees are believed to be due with this Amendment. If there are any charges associated with this filing, the Honorable Commissioner for Patents is hereby authorized to charge Deposit Account #18-2011 for such charges.

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